BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI, HYDERABAD CAMPUS
INSTRUCTION DIVISION, FIRST SEMESTER 2012-13
COURSE HANDOUT (PART-II)

Date: 03/08/2012

In addition to Part I (General Handout for all the courses appended to the time table), this portion gives further specific details regarding the course.

Course No.	**CS F215/EEE F215/ECE F215**
Course Title	**Digital Design**
Instructor-in-charge	S. K. Sahoo
Team of Instructors	
(i) For Lecture	S. K. Sahoo
(ii) For Tutorial	S. K. Sahoo
(ii) For Practical	S. K. Sahoo, Narayan K, Prasant Kumar Pattnaik
Course Description	This course covers the topics on Boolean Algebra & logic minimization; combinational logic circuits : arithmetic circuit design, Design using MSI components; Sequential Logic Circuits : flip flops & latches, registers and counters, Finite state machine; HDL Implementation of Digital circuits; Digital Integrated Circuits ; Programmable logic devices; Memory organization ; Algorithmic State machine; Introduction to computer organization; The course will also have laboratory component on digital design
Scope and Objective	The objective of the course is to impart knowledge of the basic tools for the design of digital circuits and to provide methods and procedures suitable for a variety of digital design applications. The course also introduces fundamental concepts of computer organization. The course also provides laboratory practice using MSI devices.

Text Books. :

T1: M.Moris Mano and Michael D. Ciletti " Digital Design", PHI, 4th Edition, 2007

T2: G Raghurama, , TSB Sudharshan " Introduction to Computer Organization. EDD notes 2007

T3: G Raghurama, S & Others Experiments in Digital Electronics, EDD notes 2007.

Reference Books:

R1: Donald D. Givonne ., "Digital Principles and Design" TMH, 2003

Course Plan.

Lect. No.	Learning Objectives	Topics to be covered	Reference to Text Book
1	Introduction to Digital Systems and Characteristics of Digital ICs.	Digital Systems, Digital ICs	1.1; 1.9; 2.3, 10.1,2
2.	Boolean algebra and logic gates, Codes number systems	Boolean functions Canonical forms, number systems and codes	1.2-7, 2.4-2.9
3-5	Simplification of Boolean functions	K-Maps (4,5 variables), QM Method	3.1 to 3.8
6	Simulation and synthesis basics	Hardware Description Language	3.11
7-9	Combinational Logic, Arithmetic circuits	Adders, Subtracters Multipliers	4.1 - 4-7
10-11	Sequential Logic	Flip-Flops & Characteristic tables, Latches.	5.1 to 5.4
12-14	Digital Integrated Circuits	TTL, MOS Logic families and their characteristics	10.3, 10.5, 10.7 to 10.10
15-16	MSI Components	Comparators, Decoders, Encoders, MUXs, DEMUXs	4.8 to 4.11
17	Simulation of Combinational Logic Functions.	HDL for Combinational Logic	4.12
18-20	Memory and PLDs	RAM, ROM, PLA, PAL	7.2, 7.5 to 7.7
21-22	Clocked Sequential Circuits	Analysis of clocked sequential circuits, state diagram and reduction	5.5, 5.7
23	Simulation of Sequential Logic Functions.	HDL for Sequential Logic	5.6
24-25	Registers & Counters	Shift registers, Synchronous & Asynchronous counters	6.1 to 6.5
26-27	Analysis of arithmetic units	Multiplication & Division algorithms	T2: Appendix A
28-31	Modular approach for CPU Design	RTL, HDL description	8.1,8.2, 8.4 to 8.8
32-34	Design of Digital Systems	Algorithmic State Machines	R1. Chapter 8
35-37	Design of Asynchronous Circuits.	Asynchronous Sequential Logic	9.1 – 9.4
38-40	Memory Organization	Memory Hierarchy & different types of memories	T2: Ch 6

Evaluation Scheme:

Component	Duration	Maximum Marks	Date & Time	Remarks
Test 1	60 mins	50	21/9 2.00-3.00pm	
Test 2	60 mins	50	2/11 2.00-3.00pm	
Comprehensive Examination	3 Hrs	120	5/12 AN	
Practicals: Regularity, Lab reports		40	To be announced	To be announced
Lab test & Viva/assignment		40	To be announced	

(b) Practicals (From T3.)

S.No.	Name of experiment
1.	FAMILIARIZATION OF BENCH EQUIPMENTS
2.	IMPLEMENTATION OF BOOLEAN FUNCTIONS USING LOGIC GATES
3.	OPERATION OF 4-BIT COUNTER
4.	ADDERS AND SUBTRACTORS
5.	BCD ADDER
6.	DECODERS, MULTIPLEXERS AND DEMULTIPLEXERS
7.	LATCHES & FLIP-FLOPS
8.	COMPARATORS & ARITHMETIC LOGIC UNIT
9.	COUNTERS
10.	SHIFT REGISTERS
11.	SEQUENTIAL CIRCUITS
12.	MEMORIES AND FPGAs

Make-up Policy: There will no make-ups unless for genuine reasons. Prior permission is to be taken.

Chamber Consultation Hour: To be announced in class

Notices: All notices will be posted on eduCAN only.

Instructor-in-charge,
CS F215/EEE F215/ECE F215