BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
HYDERABAD CAMPUS
COMPUTER SCIENCE & INFORMATION SYSTEMS
FIRST SEMESTER 2013 - 2014
COURSE HANDOUT (PART II)

Date: 01 / 08 / 2013

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : **CS F342**
Course Title : **Computer Architecture**
Instructor-in-charge : **Digambar Powar**
Instructors : Sanjeet Kumar Nayak
Email : powar.d@hyderabad.bits-pilani.ac.in

1. Scope and Objective:

This course aims at introducing the concept of computer architecture. It involves design aspects, and deals with the current trends in computing architecture. System resources such as memory technology and I/O subsystems needed to achieve proportional increase in performance will also be discussed.

2. Text Book:

(T1) Patterson,D.A. & J.L. Hennessy, Computer Organization and Design, Elsevier,4th ed.,2009
(T2) Samir Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, Pearson Education, Asia, 2003.

3. Reference Books:

(i) William Stallings, *Computer Organisation & Architecture*, Pearson, 8th ed., 2010.
(ii) Hamacher et. al, *Computer Organisation*, McGraw Hill, 5th ed., 2002

4. Course Plan:

Lecture No.	Topics to be covered	Reference to T1
01, 02	Introduction	Ch. 1
03, 04, 05	MIPS Architecture & Instruction Set	Ch. 3
06	Computer Arithmetic	Ch. 4.1 – 4.7
07,08	Floating Point Arithmetic	Ch 4.8 – 4.12
09, 10	Role of Performance	Ch. 2
11,12, 13	Data path Design	Ch. 5.1 – 5.3
14, 15	Control Hardware	Appendix – C
16, 17, 18	MCI, Exceptions & Microprogramming	Ch. 5.4 – 5.7
19, 20	Memory Organisation- Introduction	Ch. 7.1-7.3
21, 22	Cache Memory Organisation	-do-
23, 24, 25	Main Memory & Interleaving	Ch. 7.4 – 7.9
26, 27	I/O Organisation	Ch. 8
28, 29	Pipelining – Design Issues	Ch. 6.1 – 6.3
30, 31	Data Hazards	Ch. 6.4 – 6.5
32, 33	Control Hazards	Ch. 6.6

34, 35	Static Branch Prediction	-do-
36	Dynamic Branch Prediction	-do-
37	Advanced Concepts in pipelining	Ch. 6.8
38, 39	Modern Processors	Class Notes
40, 41, 42	Parallel Processing	Ch. 9

5. Evaluation Scheme:

EC No.	Evaluation Component	Duration (min)	Weightage (%)	Date, Time & Venue	Nature of Component
1	Test I	60	20	28/9 ,8.00 -- 9.00 AM	Closed Book
2	Test II	60	20	11/11, 8.00 -- 9.00 AM	Closed Book
3	Assignments, Lab**	-----	25		Open Book
4	Comprehensive	180	35	07/12 ,2.00 – 5.00 PM	Closed Book

** Text book **T2** will be used for Lab Assignments.

6. Chamber Consultation Hours: To be announced in the class

8. Notices: Notices regarding the course will be put up on the CSIS notice board and CMS.

9. **Makeup Policy:** No makeup exam allowed without prior permission.

Instructor - in - charge
CS F342