Birla Institute of Technology & Science, Pilani, Hyderabad Campus
Instruction Division, Second Semester 2012-2013
Course Handout: Part-II

Date: 8/1/2013

In addition to Part-I (General Handout for all courses appended to the Time-Table) this document provides specific details regarding the course.

Course No.: **(CS/ECE/EEE) F 241**
Course Title: **Microprocessors & Interfacing**
Instructor-In-Charge: **Murti KCS**
Instructors (Tutorials): **K Gopala Krishna, Rakhee, T Haripriya, V Srihari**

1. Objective:

To introduce the students with Micro Processor (MP) based system design which includes hardware, software and interfacing. After completing this course, the student should be able to design a complete MP based system for a real-world application.

2. Scope:

The course introduces the hardware components which are building blocks for MP based hardware design. Basic processor architecture will be introduced in a processor-neutral way. Programmers model of 80X86 and its architecture will be dealt in detail. Programming in Assembly language for standard program structures and embedded applications will be dealt.. Hardware design includes; basic processor based hardware design and interfacing with other peripheral devices. Interfacing to external devices , event handling through interrupts and DMA will be covered. Complete system design will be taken up as lab exercises and tutorials.

3. Course Description:

Review of digital electronics, Basic digital components for processor based design. Generic processor architecture. Microprocessor (MP) evolution. 80X86 architecture. Programmers model of 8086. Instruction set, Register set, timing diagrams. Modular assembly programming using procedures & macros. Assembler, linker & loader concepts. Concept of Interrupts: Hardware interrupts, Software interrupts. Hardware design. Memory , IO interfacing, Timing diagrams. Peripheral interfacing. Programmable I/O Devices such as 8255, 8254, 8259 etc. System design case studies. Testing and debugging of MP based systems, recent trends.

4. Text Books:

T1 : Brey Barry B. & C R Sarma The Intel Microproc,: Arch, Prog. & Interfacing Pearson Edu., 8th Edition, 2008

5. Reference books:

[R1] The x86 processors, Architecture, programming and interfacing. Lyla B Das, Pearson 2010
[R2] Morris Mano, Digital Design ,PHI, EE edition
[R3] 8086_family_Users_Manual, Intel corporation.

6. Course Plan:

a. Course Modules & Learning Objectives

Module	Title	No of classes	Learning Objectives
1	Digital design-Overview	3	Review of basic digital devices needed for processor based design. Ground work to appreciate processor based design.
2	Micro processors-architecture	6	Learn evolution of microprocessors and generic architecture of MPs.
3	80x86 architecture	4	Learn specifics of 80x86 architecture and addressing modes.

4	Programmers model and assembly programming.	9	Learn Programmers model of 80X86 and program using ASM86
5	Interrupts	3	Learn event handling through hardware and software interrupts. Real time examples.
6	Timing and hardware design	6	Learn how to analyze timing diagrams and design considerations of time in hardware design.
7	Device interfacing.	6	Learn parallel, serial, analog interfacing techniques.
8	Direct memory access	2	Learn DMA concept, DMA controller and interfacing.
9	Case studies, test tools	4	Learn complete system design and get exposed to test tools.
10	Advances	1	Very limited exposure to advanced processors in 80X86 family.

Lecture Schedule

Module	Lectures	Topics	Reference (Sections from text book)
1	1	Prelude, Number systems,	R2
	2	Basic digital devices	R2
	3	Basic digital devices-contd	R2
2	4-5	Micro computer components.	T1
	6-7	Component communication. Bus concept.	T1
	8-9	Typical instruction execution cycle	T1
3	10-11	80x86 Architecture	T1
	12-13	Addressing modes	T1
4	14-15	Assembly language programming	T1
	16	Assembly directives	T1
	17-18	Data and program control instructions	T1
	19	Arithmetic and Logical instructions	T1
	20	String instructions	T1
	21-22	Procedures	T1
5	23	Interrupts, Interrupt types, Vector tables	T1
	24-25	Event management with interrupts, Priority Schemes	T1
6	26-27	Memory & I/O Interfacing, Odd and even banks	T1
	28	Hardware architecture 8086	T1
	29-30	Instruction Cycle, Machine cycles, T- states, wait states	T1,R3
	31	Complete hardware design example	T1
7	32-33	8255 – Parallel interface	T1
	34	8254- Programmable timer interface	T1
	35-36	8259-Programmable interrupt controller interface.	T1
	37	Analog to digital conversion. ADC interface	
8	38	Direct memory access concept	T1
	39	8237-DMA interface	T1
9	40-41	Case study -1	
	42	Case study -2	
10	43	Tools-logic analyzer ,emulator	Product guides
11	44	Advances	Product guides

4. Evaluation Scheme:

Evaluation Component	Type	Duration	Weight	Date	Venue
Test 1	Open book	1-hour	20%	23/2, 5.00 - 6 .00 PM	
Test 2	Open Book	1-hour	20%	1/4, 5.00 - 6 .00 PM	
Comprehensive Exam	Closed/Open Book	3 hours	40%	14/05 FN	

Practical/Assignments			20%		

5. Assignments will include the following components:
   (a) Problem Identification, Specification, and Use Cases.
   (b) Hardware design
   (c) Programming
   (d) Prototype Implementation

6. Make-up Policy:
   Prior Permission of the Instructor-in-Charge is required to take a make-up for any component. A make-up test shall be granted only in genuine cases

7. Chamber Consultation Hour: To be announced in the class.

8. All notices shall be displayed only on the EEE NB.

Instructor-in-Charge
(ECE/EEE/CS) F241